

Implementation of Unsigned Multiplier using Efficient Carry-Select Adder for DSP Applications

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Abstract

Multiplications and additions are most widely used arithmetic computations performed in all digital signal processing applications. Addition is the basic operation for many digital applications. The aim is to develop area efficient, high speed and low power devices. Accurate operation of a digital system is mainly influenced by the performance of the adders. Multipliers are also very important component in digital systems.

This paper deals with the implementation of the VLSI design of the unsigned integer shift and add multiplier using modified carry select adder technique. The ordinary carry look ahead adder based multiplier needs the delay time of 100 ns for the multiplication. In CSLA the area is reduced to 31 % than in the CLAA based multiplier. The Conventional CSLA based multiplier uses the delay time of 100 ns for performing multiplication operation where as in modified CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area and power needed for CSLA multiplier is reduced by the modified CSLA based multiplier to complete the multiplication operation.

The proposed 32-bit modified CSLA design consumes 16159.38 nW power and 298 μm^2 area. The proposed 64-bit modified CSLA design consumes 33417.16 nW power and 692 μm^2 area. The proposed 16-bit Multiplier using modified CSLA design consumes 18093.64 nW power and 993 μm^2 area. The proposed 32-bit Multiplier using modified CSLA design consumes 22793.293 nW power and 1868 μm^2 area. After implementing 16-bit proposed Multiplier design, the area occupied is 298 LUT's which is reduced by 16.27 % than 16-bit existing Multiplier which occupied 692 LUT's and power is reduced to 18093.64 nW. After implementing 32-bit proposed Multiplier design, the area occupied is 493 LUT's which is reduced by 14.49 % than 32-bit existing Multiplier which occupied 986 LUT's and power is reduced to 22793.293 nW.

Key Words: Area, Power, CSLA, Adder, Multiplier

1. INTRODUCTION

Low-power, area-efficient and high-performance VLSI systems are increasingly used in portable devices, mobile devices, multi-standard wireless receivers, and bio-medical instrumentation. Digital computer arithmetic is one of the main features of logic design with the aim of developing appropriate algorithms in order to optimize the utilization of the available hardware. Hardware can only perform a simple and limited set of operations. Multiplication is the basic arithmetic operation which is present in many part of the digital computer especially in computation system. It requires substantially more hardware resources and processing time than addition and subtraction. In fact 8.72% of all the instructions in typical processing units are multiplication. An area efficient, fast and accurate operation of the multiplier is mainly influenced by the performance of the adder [1].

Scope of project is to design and implement a modified Carry Select Adder (CSLA) replacing Conventional Carry Select Adder design in the Add Shift multiplier design to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. The proposed system will be addressing this problem. The key contribution in this work is to come up with a more efficient and low power

architecture than the existing design which provides better performance such as area and power consumption.

The area and power consumption of the regular CSLA architecture can be reduced by using BEC instead of the Ripple Carry Adder (RCA) with $C_{in} = 1$. Logic gates are reduced in this architecture and delay is less. The basic function of the CSLA is derived by using the 4-bit BEC together with the multiplexer. The input of 8:4 multiplexer is B3, B2, B1, and B0 and another input is BEC output. The two possible partial results are produced in parallel and multiplexer select either the BEC output or the direct input depends on control signal. The advantage of the BEC logic is the larger area reduction when the CSLA with large number of bits are designed. The reduced number of gates offers the great advantage in the reduction of area and also the total power [2].

The carry select adder divides the adder into different groups. Each group performs two additions in parallel. Two ripple-carry adder acts as carry evaluation block at select stage. One RCA evaluates the carry chain with carry in is zero, while other assumes it as one. Once the carry signal is obtained, the multiplexer is used to select the final carry out signal. This results in reduced power dissipation, less area and with no degradation in speed [3]. The main disadvantage of the regular CSLA is the doubling of the area cost to duplicate architecture. The architecture of Conventional CSLA adder comprises a single RCA, a first

zero detection and complement add-one circuit, and a multiplexer circuit is comparatively effective than using dual RCAs in conventional CSLA.

The adder structure is partitioned into blocks of consecutive stages with a ripple-carry. Each block generates a carry propagate signal that equals one if all internal stages satisfy $P_m = 1$. This propagate signal allows an incoming signal to skip and generate a carry output. Figure 3.4 shows an example carry skip adder blocks. The carry skip adder is linear in the number of bits N. The slope of the delay increases in gradual fashion than ripple-carry adder. Ripple-carry adder is fastest for small values of N. The cross point is 4-8-bits between the ripple-carry adder and carry skip adder [4].

The designing of carry look adder has its advantage that it first calculates all carry bits after it calculates the sum bits. Carry look ahead adders are used in time critical applications to calculate fast results and the limitations of carry look ahead adder is it leads to increase in area [5]. This paper deals with an area-efficient carry select adder by sharing the Common Boolean Logic (CBL) term. By sharing the common boolean logic term, the duplicated adder cells can be removed in the conventional carry select adder. After logic simplification and sharing partial circuit, we only need one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. In this way, the transistor count in a 32-bit carry select adder can be greatly reduced moreover; the power consumption can be reduced from as well as power delay product can be reduced. By retaining part of parallel architecture of conventional carry select adder, we can still maintain some competitiveness in speed. In this way, our area-efficient adder can perform with nearly the same transistor count, nearly the same power consumption, but with faster speed and lower power delay product as compared with the carry adder [4].

2. CONVENTIONAL CSLA

The CSLA is mainly partitioned into two units: sum and carry generator unit (SCG) and sum and carry selection unit (SCS). The SCG unit consumes most of the logic resources of CSLA and contributes significantly to the critical path. Different logic design has been suggested for efficient implementation of SCG unit. Study on the logic designs are carried out for SCG unit of conventional CSLA and CSLA-BEC by suitable logic expressions. The main objective of this study is to identify redundant logic operations and data-dependency. Fig. 1 and Fig. 2 shows the Conventional CSLA and BEC based CSLA.

2.1 Logical Expressions

As shown in Fig. 1, SCG unit of conventional CSLA is comprised of two n-bit RCA's, where n is the adder bit width. The logic operation of n-bit RCA is performed in four stages:

- Half-Sum Generation (HSG)
- Half-Carry Generation (HCG)
- Full-Sum Generation (FSG)
- Full-Carry Generation (FCG)

$$\begin{aligned}
 s_0^0(i) &= A(i) \oplus B(i); & c_0^0(i) &= A(i) \cdot B(i) & \dots & \text{i} \\
 s_1^0(i) &= s_0^0(i) \oplus c_1^0(i-1) & & & \dots & \text{ii} \\
 c_1^0(i) &= c_0^0(i) + s_0^0(i) \cdot c_1^0(i-1); & c_{out}^0 &= c_1^0(n-1) & \dots & \text{iii} \\
 s_0^1(i) &= A(i) \oplus B(i) & c_0^1(i) &= A(i) \cdot B(i) & \dots & \text{iv} \\
 s_1^1(i) &= s_0^1(i) \oplus c_1^1(i-1) & & & \dots & \text{v} \\
 c_1^1(i) &= c_0^1(i) + s_0^1(i) \cdot c_1^1(i-1); & c_{out}^1 &= c_1^1(n-1) & \dots & \text{vi}
 \end{aligned}$$

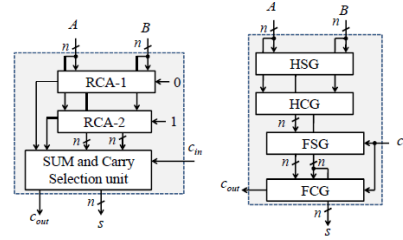


Fig. 1 Conventional CSLA

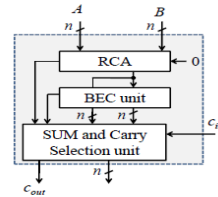


Fig. 2 BEC based CSLA

In Fig. 2, the RCA calculates n-bit sum s_0 and c_{out} corresponding to $c_{in}=0$. The BEC unit receives s_0 and c_{out} from the RCA and generates $(n + 1)$ -bit excess-1 code. The most significant bit of BEC represents c_{out} , where n LSBs represent s_1 . A logic expression of RCA is the same as those given in conventional CSLA RCA. Logic expressions of BEC unit of n-bit CSLA-BEC are

$$\begin{aligned}
 s_1^1(0) &= \overline{s_0^0(0)}; & c_1^1(0) &= s_0^0(0) & \dots & \text{i} \\
 s_1^1(i) &= s_0^0(i) \oplus c_1^1(i-1) & & & \dots & \text{ii} \\
 c_1^1(i) &= s_0^0(i) \cdot c_1^1(i-1); & & & \dots & \text{iii} \\
 c_{out}^1 &= c_0^1(n-1) \oplus c_1^1(n-1) & \dots & \text{iv}
 \end{aligned}$$

3. MODIFIED ADDER BLOCK

The Modified Adder block (Fig. 3) consists of four units:

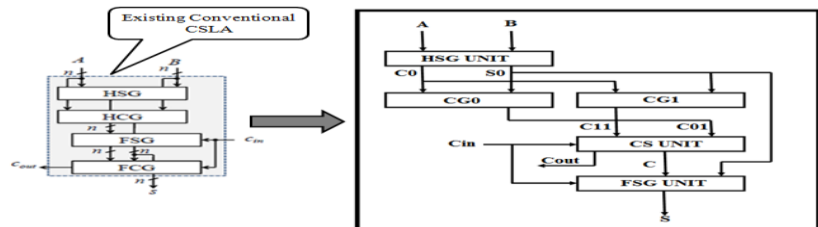


Fig. 3 Modified adder block

- Half Sum Generator Unit (HSG)
- Carry Generator Unit (CG)
- Carry Select Unit (CS)

- Full Sum Generator Unit (FSG)

All the redundant logic operations of Conventional CSLA and BEC based CSLA are removed and rearranged the logic expressions based on their data dependency. The Advantages of modified adder blocks are,

- Calculation of s01 is avoided in the SCG unit
- n-bit select unit is required instead of (n + 1)-bit
- Less output-carry delay

4. MULTIPLIER DESIGN

The requirement is to implement a 16*16-bit multiplier based on the shift and add method. The overall architecture is shown in Fig. 4. The multiplier shall accept the inputs 16-bit multiplier and 16-bit multiplicand as well as a Start signal.

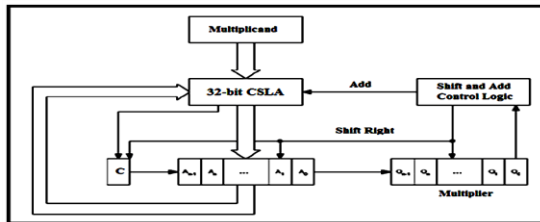


Fig. 4 Add-Shift multiplier block diagram

5. APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) IMPLEMENTATION

5.1 Area and Power of Proposed Adders Architecture

The RTL design is synthesised with by using RTL Compiler. In turn the tool synthesized the design using the target library was a low power 65 nm (tcbn65lphvtwc) and generated the netlist. Upon analysing, elaborating and compiling the designs, constrained by a given clock period and obtained area and power estimates are shown in Table 1 and 2.

Table 1 Area Report of Proposed Adder

Adders	Area (μm^2)
16-Bit Proposed CSLA	298
32-Bit Proposed CSLA	692

Table 2 Power Report of Proposed Adder

Adders	Power (nW)
16-Bit Proposed CSLA	16159.38
32-Bit Proposed CSLA	33417.16

5.2 Area and Power of Proposed Multiplier Architecture

The RTL design is synthesized using RTL Compiler. In turn the tool synthesized the design using the target library

was a low power 65 nm (tcbn65lphvtwc) and generated the netlist. Upon analysing, elaborating and compiling the designs, constrained by a given clock period and obtained area and power estimates are shown in Table 3 and 4.

Table 3. Area Report of Proposed Multiplier

Multipliers	Area (μm^2)
16-Bit Multiplier using Modified CSLA	993
32-Bit Multiplier using Modified CSLA	1868

Table 4. Power Report of Proposed Multiplier

Multipliers	Power (nW)
16-Bit Multiplier using Modified CSLA	18093.64
32-Bit Multiplier using Modified CSLA	22793.293

6. RESULTS COMPARISON

6.1 Comparing Area and Power report of Proposed and Existing adders

The proposed 32-bit modified CSLA design consumes 16159.38 nW power and 298 μm^2 area. The Proposed 32-bit existing conventional CSLA design consumes 35691.08 nW power and 493 μm^2 area. The Proposed 32-bit modified CSLA design involves 39.5% of less area and 54.7% of less power consumption than the 32-bit Conventional CSLA. Fig. 5 shows the comparison chart of 32-bit proposed and existing adder.

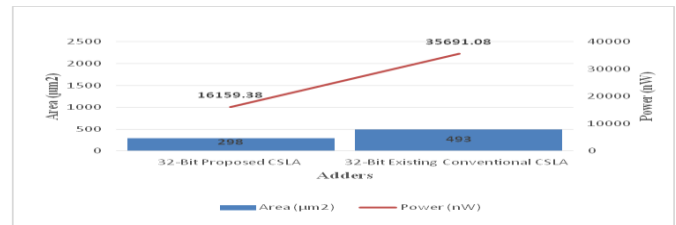


Fig. 5 Comparison chart of 32-bit proposed and conventional CSLA

6.2 Comparing Area and Power report of Proposed and Existing adders

The proposed 64-bit modified CSLA design consumes 33417.16 nW power and 692 μm^2 area. The 64-bit existing conventional CSLA design consumes 70739.69 nW power and 986 μm^2 area. The Proposed 64-bit modified CSLA design involves 29.8% of less area and 52.7% of less power consumption than the 64-bit Conventional CSLA. Fig. 6 shows the comparison chart of 64-bit proposed and existing adder.

6.3 Comparing Area and Power report of 16-bit Multipliers

The proposed 16-bit Multiplier using modified CSLA design consumes 18093.64 nW power and 993 μm^2 area.

The 16-bit multiplier using existing conventional CSLA design consumes 19692.351 nW power and 1186 μm^2 area. The Proposed 16-bit multiplier using efficient adder design involves 16.27% of less area and 8.1% of less power consumption than the 16-bit multiplier using Conventional CSLA. Fig. 7 shows the comparison chart of 16-bit proposed and existing multiplier.

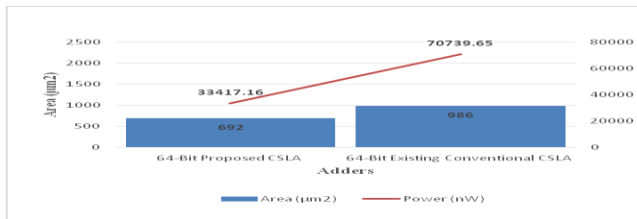


Fig. 6 Comparison chart of 64-bit proposed and conventional CSLA

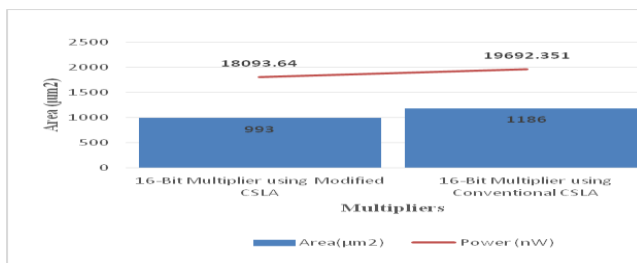


Fig. 7 Comparison chart of 16-bit proposed and existing multiplier

6.4 Comparing Area and Power report of 32-bit Multipliers

The proposed 32-bit Multiplier using modified CSLA design consumes 22793.293 nW power and 1868 μm^2 area. The 32-bit Multiplier using existing conventional CSLA design consumes 22921.06 nW power and 2264 μm^2 area. The Proposed 32-bit multiplier using efficient adder design involves 14.49% of less area and 0.5% of less power consumption than the 32-bit multiplier using Conventional CSLA. Fig. 8 shows the comparison chart of 32-bit proposed and existing Multiplier.

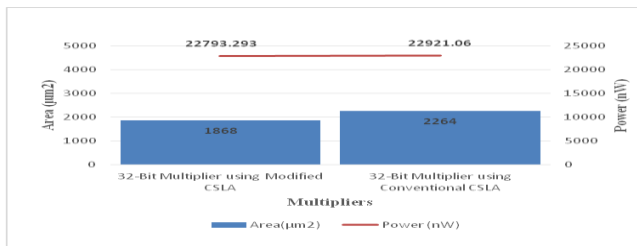


Figure 10 Comparison chart of 32-bit proposed and existing multiplier

7. CONCLUSIONS

The proposed 32-bit modified CSLA design consumes 16159.38 nW power and 298 μm^2 area. The proposed 64-

bit modified CSLA design consumes 33417.16 nW power and 692 μm^2 area. The Proposed 16-bit Multiplier using modified CSLA design consumes 18093.64 nW power and 993 μm^2 area. The proposed 32-bit Multiplier using modified CSLA design consumes 22793.293 nW power and 1868 μm^2 area.

The proposed 32-bit modified CSLA design resulted in 39.5% of reduced area and 54.7% of reduced power consumption than the 32-bit Conventional CSLA. The proposed 64-bit modified CSLA design involves 29.8% of reduced area and 52.7% of reduced power consumption than the 64-bit Conventional CSLA. The proposed 16-bit multiplier using efficient adder design involves 16.27% of reduced area and 8.1% of reduced power consumption than the 16-bit multiplier using Conventional CSLA. The proposed 32-bit multiplier using efficient adder design involves 14.49% of reduced area and 0.5% of reduced power consumption than the 32-bit multiplier using Conventional CSLA.

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