Design and Simulation of an Optical AND and XOR Gate using Micro Ring Resonator for Photonic FPGA

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Abstract

Silicon photonics is an innovative technology that revolutionizes a number of domains such as data centres, high-performance computing, sensing and Field Programmable Gate Array (FPGA). The photonics based digital devices are utilized in low space and low power. Very Large Scale Integration (VLSI) designs pave ways for future photonics FPGA. Logic gates are the basic element for combinational and sequential models. The existing architecture used for the development of AND & XOR gates have more number of Micro Ring Resonators (MRRs) and consume a lot of space. In this paper design and simulation of XOR and AND logical devices using an optical MRR and Electro-optic effect has been explained. Electrical voltage source has been used as external input to achieve electro optic effect. A compact XOR and AND gate has been designed and can be easily fabricated using existing foundries. The designed and simulated XOR & AND logical devices occupies space of 500 μm² and consumes a power of 13.18 μW.

Key Words: Optical Waveguides, XOR Gate, AND Gate, Micro Ring Resonator (MRR), Very Large Scale Integration (VLSI)

1. INTRODUCTION

Photonics, the science and technology of generating, controlling, and detecting light, is rapidly growing into mainstream electronic designs. Photonic Integrated Circuits (IC) comes with some unique challenges in areas including layout, error checking, and circuit modelling. High speed communication and data transfers are playing a key role in growing technologies, such as medical, aerospace and defense. VLSI plays a major role in terms of manufacturing of high speed, low power processors, system-on-chips (SOC's) and programmable IC's. Existing CMOS transistor technology has upgraded till 7 nm to reduce the power and increase the speed and performance. Even though the emerging technologies such as fin-FET, CNT-FET [1] Can still improve the speed and performances, they are limited due to speed and power boundaries. Photonics is the state of art technology to satisfy the above stated constraint of the existing technology. Integrated photonics technique has been used to develop a logical architecture and is composed of two silicon micro ring resonators capable of operating XOR and AND [2]. The micro ring resonators are modulated by thermo-optic action and the optical AND logic gate is experimentally demonstrated in a single silicon micro ring resonator. The architecture used for AND gate and XOR gate are different which consists of optical ring resonators. Symmetry and change in refractive index property of the micro-ring resonator is used to build the logic gates. Logic gates are the basic element for a combinational and sequential models. AND and XOR gate play a very important role in Digital electronics [3]. A logic gate is a tiny transistor circuit, essentially a type of amplifier that is implemented in various forms in an integrated circuit. Logic gates are used to make a few combinational circuits like multiplexers, demultiplexers, encoders, decoders etc. and also a few arithmetic circuits such as adders, subtractors, comparator etc. Arithmetic Unit and Logic Unit can constructed using logic gates. The flip-flops, counters and registers are made to store data. Registers, RAM, ROM etc. are constructed with these logic gates. However ROM can be implemented using decoders and multiplexers too. Interfacing them in a proper manner gives a processing unit. Such processors are the heart of cell phones, laptops and similar digital devices.

1.1 Background and Related Work

A concept called Silicon-On-Insulator (SOI) [4] is mainly used in silicon photonics, in which silicon is placed on the top of silica layer [5]. An optical device called Micro-Ring Resonator (MRR), is a symmetrical device having one ring waveguide and two straight waveguides to provide a coupling of light between them. Ring resonator works on two basic concepts of light i) Constructive Interference ii) Total Internal Reflection. MRR has four ports named as Input, Through, Add and Drop ports. Output is measured at drop port as shown in Fig. 1.

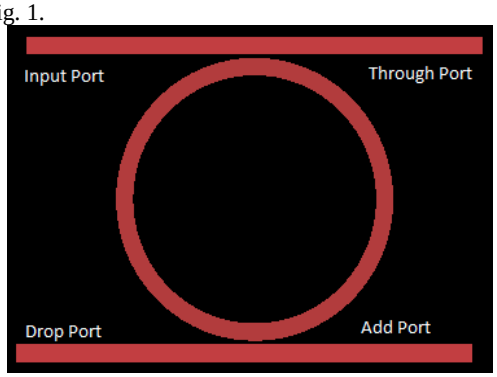

Fig. 1 Dual waveguide Micro-Ring resonator

Electro-optic effect is the significant phenomenon used for electro-optic modulation. Electro-optic effect is created by forming a PN junction around the ring, which is equivalent to PN diodes. Applying a voltage to the PN junction ring resonator [6] causes the variations in the electron and hole densities which in turn changes the refractive index of the ring resonator. The change in the refractive index shift the wavelength at the output port (drop port).

An all-optical AND logic gate using a single silicon microring resonator is experimentally demonstrated with an architecture called Four Wave Mixing (FWM.) Two wavelengths, λ_1 and λ_2 are given as input source to the microring resonator, field-enhanced FWM (interactions between two or three wavelengths produce two or one new wavelengths) takes place in the ring, resulting in the generation of a new wavelengths whose intensity follows the logic operation between the inputs [7]. The XOR gate architecture is based on Si_3N_4 platform [8]. A XOR and XNOR logic gate based on microring is discussed, which uses thermo-optic impact and electrical pumping for operation. The design comprises of 15 microring resonators, in which each MRR is identical to one another and its specifications are same. All the connectivity in XOR and AND gate is done using copper (Cu) materials. Copper materials have some amount of wire delays which causes latency in this architecture.

1.2 Design and Simulation of Optical AND and XOR gate

In the existing design of optical AND and XOR gate a delay of 5.48 $\frac{ns}{m}$ has been observed [9]. The existing architecture for optical AND and XOR gate uses multiple wavelength which depends on a number of inputs and the area occupied is 10000 µm². The proposed logic module performs various arithmetic and logical operations for different combinations of input bits with the addition of one or two beam combiners. It performs logical operation namely AND and XOR. The proposed design can be configured as a half adder and a half subtractor [8]. Power of 13.18 µW is achieved and speed up to 588.878 THz is achieved, since it has optical waveguides. Only three wavelengths are used to interpret the logic states. Finally the space used is 500 µm².

A. Micro-Ring Resonator Design

Ring resonator has various parameters, which is very important in design. They are, radius of the MRR, height/thickness of the waveguide (core and cladding), width of the straight waveguides, air gap between the waveguide and ring, materials used. These parameters are important for finding effective refractive index (neff) and relation between the ring radius, wavelength and neff, which is given by equation (1);

$$m\lambda = 2\pi n_{eff} R \quad (1)$$

where m is the mode number, λ represents the wavelength to be used for the design (1.55µm), n_{eff} is the material-dependent efficient refractive index (2.65) and R is the radius of the ring [9]. A lumerical FDTD is used to design MRR, time frequency monitor is used to measure the transmitted power and wavelength. Mode source with the input range from 1.45µm to 1.65µm is used as the light source. The designed MRR using lumerical FDTD [10] is shown in Fig 2.

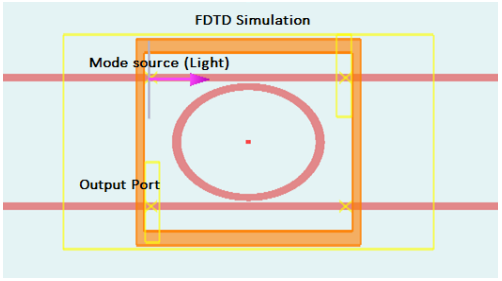

Fig. 2 Designed Micro Ring Resonator

B. Simulation of PN junction on Micro Ring Resonator

An opto-electric effect of the MRR causes the change in refractive index, which produces the shift in wavelength on spectrum [10]. The cathode and anode developed around the ring is shown in Fig 3. Cathode has P side with aluminum (Al) material, anode has N side with aluminum (Al) material, which forms a PN junction [11]. A voltage of 2V causes change in electron hole density, that produces the change in refractive index.

$$neff = F(V) \quad (2)$$

$$\Delta neff = \lambda K E^2 \quad (3)$$

In equation (2) neff is a function of applied bias, which can be represented in terms of electric field (E) as in equation (3). In equation (3) K is the kerr constant (2.7×10^{-9} mV^{-2}) [12], λ is wavelength, Δneff change in refractive index.

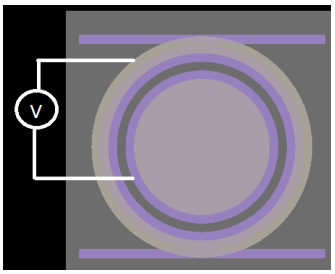

Fig. 3 PN junction on Micro Ring Resonator

PN junction [12] MRR is placed on silicon in Fig 3. SiO_2 layer is placed above the Si, and this forms SOI [13]. This substrate uses a thickness of 8µm. Since the design uses silicon, transmission losses get reduced and it is easier for fabrication using semiconductor fabrication process. [14]

C. Simulation of AND gate

AND gate uses a continuous wave architecture. On SOI wafer with a top silicon thickness of 250 nm and buried silica of 3 µm, MRR with a radius of 47 µm and a bus waveguide of 3.5 mm is developed. The height and width of both straight and ring wave guides is 540 nm and 250 nm respectively. An input is a light source of wavelength 1550 nm [15]. Because of their smaller mode volumes, MRRs with smaller radii have reduced energy demands, which also make free carriers build up quicker, resulting in enhanced nonlinear

losses and reduced Conversion Efficiency (CE). Developed logical AND gate is shown in Figure 4.

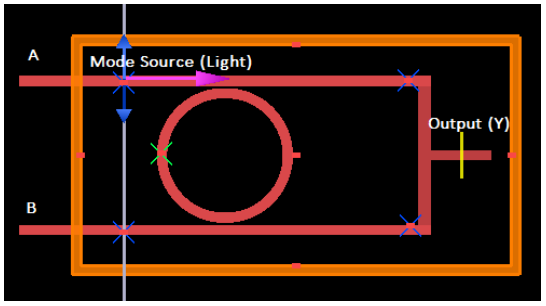

Fig. 4 Simulated Logical AND gate

Table 2. Interpretation of wavelength into logic states

Voltage Input (Wavelength)	Logic states
λ1 1.52381 µm	'0'
λ2 1.54839 µm	'1'

D. Development of XOR gate

The XOR gate design consists of 220 nm thick silicon (Si) layer silicone-on-insulator wafer and 2 µm thick buried silicon dioxide layer. The Si wave guides' cross segments are 400×220 nm^2, and the ring wave guides' radii is 10 µm each. The gaps between the waveguides of the ring and the waveguides are 400 nm. The P junction is of Aluminum material which is of 9.5 µm and N junction is a circular waveguide which also uses Aluminum material. Its radius is 8 µm. By using silicon transmission losses get reduced and it makes easy for fabrication using semiconductor fabrication process. An electro-optic modulation system is adopted as it requires a less complex structure of the device layer and therefore results in easy manufacture. Developed logical XOR gate is shown in Fig 5.

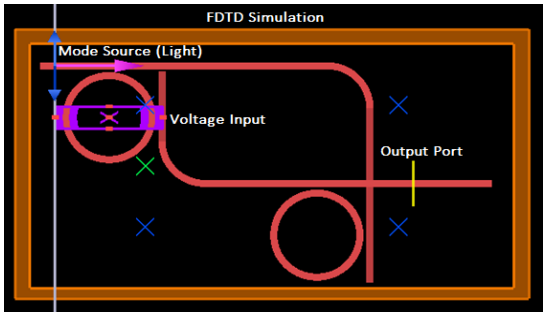

Fig. 5 Simulated Logical XOR gate

Table 3. Interpretation of wavelength into logic states

Wavelength	Logic states
Without bias voltage (0v)	'0'
With voltage (V1)	'1'
λ1 (1.54355 µm)	'00'
λ2 (1.49531 µm)	'01'

Wavelength	Logic states
Without bias voltage (0v)	'0'
With voltage (V1)	'1'
λ3 (1.59500 µm)	'10'
λ1 (1.54355 µm)	'11'

1.3 Results and Discussion

The AND & XOR gates are designed using microring resonators.

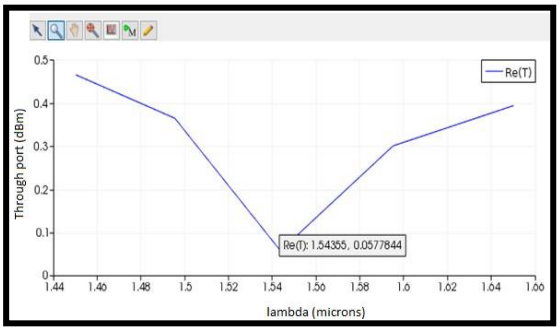

Fig. 6 Through port power versus wavelength

In Fig 6, output of a MRR is shown.

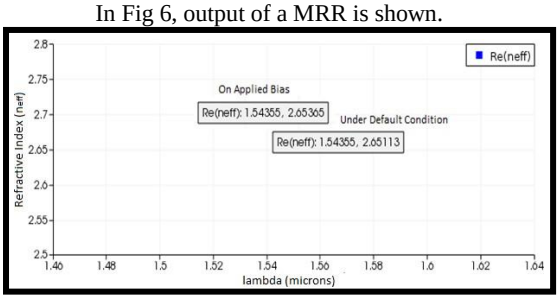

Fig. 7 Refractive index versus wavelength

In Fig 7, the refractive index is measured under two conditions. (i) Without bias (ii) With bias

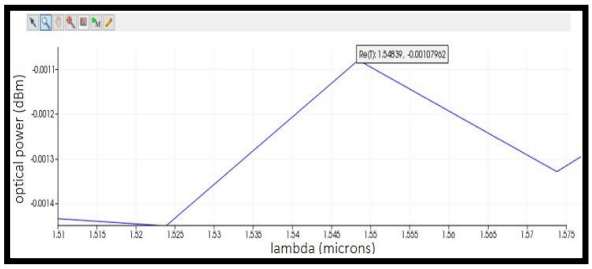

Fig. 8 Output of an AND gate when Y=1

In Fig 8, When input of A=1 and B=1, then the resultant output of an AND gate is Y=1

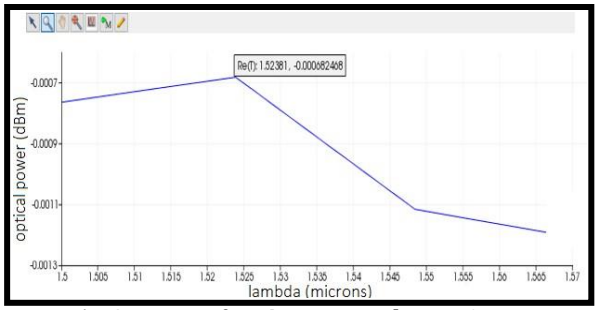

Fig. 9 Output of an AND gate, when Y=0

In Fig 9, When input of A=0 and B=0, then the resultant output of an AND gate is Y=0

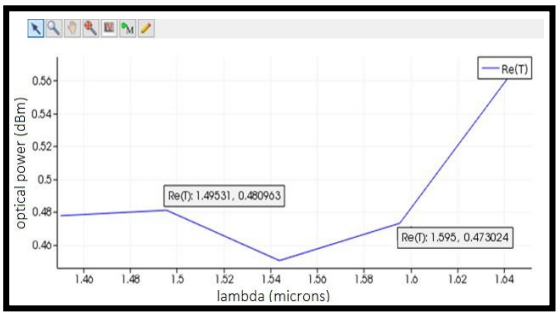

Fig. 10 Output of an XOR gate, when Y=0

In Fig 10, When input of A=0 and B=0, then the resultant output of an XOR gate is Y=0

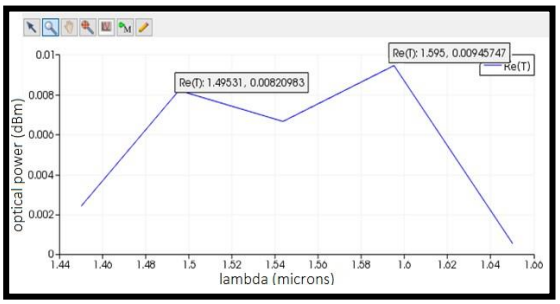

Fig. 11 Output of an XOR gate, when Y=1

In Fig 11, When input of A=0 and B=1, then the resultant output of an XOR gate is Y=1

2 CONCLUSION

A compact optical logical AND & XOR gates is proposed using micro ring resonator. The designed AND & XOR gates occupies space of 500μm^2 and power of 2.7x10^{-11} W. The designed geometry of AND & XOR gates has been chosen in such a way that it can be fabricated with currently available foundries.

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