# DESIGN AND FPGA IMPLEMENTATION OF RECONFIGURABLE DIGITAL FRONT END MODULE OF MIMO-OFDM FOR UWB SYSTEM

**Vikram Nandyal[1], T. Vasudeva Murthy[2], R. Selva Kumar[3]**

1- (Engg.) Student, 2- Senior Training Engineer, 3- Senior Lecturer,
VLSI System Design Centre
M.S.Ramaiah School of Advanced Studies, Bangalore

## *Abstract*

*The Multi Input Multi Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) based Ultra-Wideband (UWB) systems are set to revolutionize consumer electronics, in the near future. With low power consumption, high data rates up to 480 Mbps, large spatial capacity and low interference with other wireless services due to low power spectral density, MIMO-OFDM based UWB systems are the most sought after for wireless communications. The application targeted by this design was the band 1 of 'Band group 1' based UWB system with a center frequency of 3.432 GHz and a bandwidth of 528 MHz.*

*This paper focuses on FPGA implementation of Reconfigurable Digital Frontend module of MIMO-OFDM. The modeling of the MIMO-OFDM system was carried out in MATLAB followed by Verilog HDL implementation. Unlike the conventional OFDM based systems, Numerically Controlled Oscillators (NCO) are used for mapping modulated data onto the subcarriers. The use of NCO in the MIMO-OFDM system reduces the resource utilization of the design on FPGA along with reduced power consumption. The major modules that were designed, which constitute the digital frontend module, are Quadrature Phase Shift Keying (QPSK) modulator/demodulator, 16-Quadrature Amplitude Modulation (QAM) modulator/demodulator and NCOs. Each of the modules was tested for its functionality by developing corresponding testbenches.*

*This paper has resulted in a hardware implementation of the MIMO-OFDM based UWB system on a SPARTAN 3 FPGA board. The NCO based architecture utilizes 30% of slices, 27% of 4-input LUTs, 20% of IOBs and 9% of slice Flip Flops on the SPARTAN 3 board. The NCO based architecture utilizes 70% lesser resources on the SPARTAN 3 board, than Inverse Fast Fourier Transformation (IFFT) based design. The system consumes a power of 278.48 µWatt and operates at a maximum frequency of 181.8 MHz.*

**Key Words:** Orthogonal Frequency Division Multiplexing, Ultra-Wide Band, Multi-input Multi-output, Numerically Controlled Oscillator

## Abbreviations

| | |
|---|---|
| BER | Bit Error Ratio |
| BLAST | Bell Labs Layered Space Time |
| BPSK | Binary Phase Shift Keying |
| CIC | Cascode Integrated Comb |
| D-BLAST | Diagonal Bell Layer Space Time |
| DBe | Digital Backend |
| DFe | Digital Frontend |
| FFT | Fast Fourier Transform |
| FPGA | Field-Programmable Gate Array |
| HDL | Hardware Description Language |
| ISI | Inter-Symbol Interference |
| IO | Input/Output |
| LST | Layered Space-Time |
| LUT | Look Up Table |
| MSB | Most Significant Bit |
| QPSK | Quadrature Phase Shift Keying |
| QAM | Quadrature Amplitude Modulation |
| RTL | Register transfer Logic |
| STBC | Quasi-Space Time Block Coding |
| SISO | Single-Input and Single-Output |
| STBC | Space-Time Block Code |
| SDM | Spatial Division Multiplexing |
| STTC | Space-Time Trellis Code |
| SIPO | Serial-In Parallel-Out |
| UWB | Ultra Wide Band |
| WPAN | Wide-Personal Area Network |

## 1. INTRODUCTION

UWB offers a mechanism for transporting data, audio and video wirelessly. From the time UWB came into existence, it has traversed an intriguing path from the laboratory to defense applications and back to laboratory until it was commercially launched. The development of UWB cannot be credited to just one person; in fact the technology belongs to various innovative thinkers and scientists over the last five decades. The interest in the technology has been steady based on the fact that over 200 technical papers were published in journals between 1960 and 2009 along with over 100 patents in UWB technology during the same period. Federal Communications Commission (FCC) specifications mandate that UWB radio transmission legally operates in the range from 3.1 GHz to 10.6 GHz, at a transmit power of –41 dBm/MHz [1].

Of late there has been substantial interest in the application of Multi-Input Multi-Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) for wireless communication, UWB systems in particular, due to its resilience to RF interference and lower multi-path fading. Conventional radio transmission uses one antenna at the transmitter and one antenna at the receiver. These systems are termed as Single Input Single Output (SISO) systems**.** Both the transmitter and the receiver have one RF chain (i.e., an encoder and a modulator). SISO is relatively simple and inexpensive to implement and has been used since time immemorial. To multiply throughput of a radio link, innovative techniques, such as, multiple antennas (and multiple RF chains accordingly) at both the transmitter and the receiver, have been employed. These systems are termed as MIMO systems. A MIMO system with similar count of antennas at both the transmitter and the receiver in a point-to-point (PTP) link is able to multiply the system throughput linearly with every additional antenna.

OFDM is a technique that divides a communication channel into a number of equally spaced frequency bands. A subcarrier carrying a portion of data is transmitted in each frequency band. Each subcarrier is orthogonal (independent of each other) with every other subcarrier, differentiating OFDM from the commonly used FDM. OFDM is sometimes called multi-carrier or discrete multi-tone modulation [2]. The OFDM technique is efficient at collecting multipath energy in highly dispersive channels, as is the case for most UWB channels. Moreover, OFDM allows each subband to be divided into a set of orthogonal narrowband channels (with a much longer symbol period duration) [3].

High-data-rate WPANs can be defined as networks with a medium density of active devices per room (5 to 10) transmitting at data rates ranging from 100 to 500 Mbps within a distance of 20 m. The ultra-wide bandwidth of MIMO-OFDM based UWB aides various WPAN applications. The applications such as high-speed wireless universal serial bus (WUSB) connectivity for personal computers (PCs) and PC peripherals, high-quality real-time video and audio transmission, file exchange among storage systems, and cable replacement for home entertainment systems are the beneficiaries.

MIMO-OFDM based UWB transmission can trade a reduction in data rate for an increase in transmission range. Under the low-rate operation mode, UWB technology could be potentially utilized in sensors, position tracking, and identification networks. A sensor network consists of large number of nodes spread over a geographical area to be monitored. Key requirements for sensor networks operating in extreme and challenging environments include low cost, low power, and multi-functionality. Moreover, due to the fine time resolution of UWB signals, OFDM based UWB sensing has the potential to improve the resolution of conventional proximity and motion sensors. The low-rate transmission, combined with accurate location tracking capabilities, offers an operational mode known as *low-data-rate and location tracking* [4].

The Figure 1 illustrates the simplified MIMO-OFDM based UWB system. The highlighted OFDM section in the Figure 1 represents the digital MIMO-OFDM module. The digital module in turn consists of digital backend and digital frontend MIMO-OFDM modules. This paper discusses the design and implementation of the DFe MIMO-OFDM module.

## 2. PROBLEM DEFINITION

The design of re-configurable digital frontend MIMO-OFDM module targeting UWB application in the ‘Band group 1’ of the UWB spectrum is described in this paper. The module is designed to be utilized in high data rate and low power wireless systems. This paper introduces a new NCO based architecture for mapping/de-mapping modulated data onto the sub-carriers, unlike the conventional systems which use IFFT/FFT for the same. The utilization of NCOs results in lesser resource utilization in terms of area and power, also resulting in higher frequency of operation as compared to the IFFT/FFT based architectures. The reference model of the MIMO-OFDM module was designed in MATLAB. The RTL simulation and synthesis were carried out using ModelSim and Xilinx ISE tool respectively, targeting SPARTAN 3 FPGA board. The functionality of the hardware was then verified using Chipscope Pro tool.

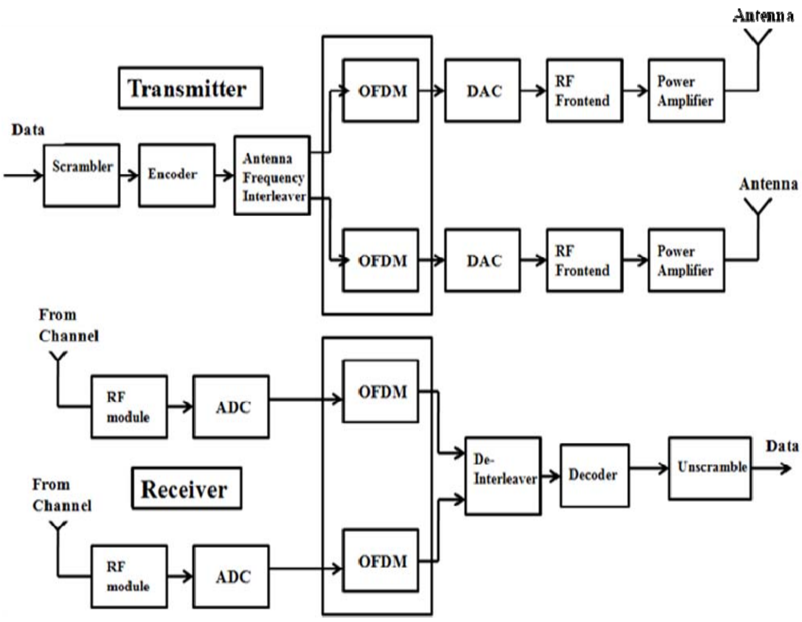


**Fig. 1 Simplified MIMO-OFDM based UWB system**

## 3. METHODOLOGY

Matthew Welborn [1] suggests that, to achieve data rates close 1.5 to 2 Gbps in 500 MHz bandwidth it would require scaling to 64-QAM, where there is a significant difference in power efficiency between QPSK and 64-QAM. For instance, the minimum Eb/N0 required at the receiver is 9.6 dB for BPSK at $10^{-5}$ bit-error rate (BER) and almost 10 dB higher for 64-QAM at the same BER. The result is that high order modulation requires higher transmit power in order to provide equivalent BER at the receiver. The tight constraints on UWB transmit power result in significant range performance differences in realistic operating conditions. When the narrower bandwidth designs are to be extended to higher rates, the use of high order modulation and multiple antenna technologies can provide scalable and robust performance, but will also likely lead to increased complexity and power consumption. Systems that use wider bandwidths, such as direct sequence UWB, can use more efficient modulation and design approaches to provide wireless connectivity solutions that scale to even higher data rates with more scalable and lower complexity implementations.

**Table 1. Design specifications of the system**

| Parameters | |
|---|---|
| IF | 500MHz |
| Number of subcarriers | 64 |
| Cyclic prefix | 16 point |
| Modulation schemes | QPSK and 16-QAM |
| Achievable data rate | 100 Mbps |
| Targeted FPGA | SPARTAN 3 |

The major drawback of the suggested architecture in [1] is the use single carrier systems against the multi carrier systems. The use of OFDM based systems results in efficient utilization of the spectrum, as compared to the single carrier systems. The use of multi carrier systems also increases the data rate with the low modulation schemes unlike the single carrier systems.

Oscar Robles Palacios and Carlos Silva Cardenas [5] suggest an architecture consisting of an oscillator based on direct digital synthesis (DDS) techniques, which is a digital control method of generating multiple frequencies from a reference clock signal [6]. This characteristic provides a system with great accuracy in terms of signal integrity. Though the DDS and the IFFT functional units differ in many ways, it is important to mention that both of them will perform the same function, which is to transfer the signal from the frequency domain to the time domain. The ideal replacement of the IFFT functional unit in OFDM implementations is a DUC (Digital Up-Converter). Using DUCs is more suitable because they contain three filters – Programmable Finite Impulse Response (PFIR), Compensation Finite Impulse Response (CFIR) and CIC, that accomplish a better spectral shaping of the signal. However, these filters increase the sample rate and delay, and require more synchronization hardware. The flexibility of the proposed design lies in the control unit of the system. The flexibility of this system lies in the Control Unit.This subsystem is in charge of analyzing the information inside the Instruction signal, and sending the appropriate orders to the rest of functional units. The four bits inside the instruction signal establish the constellation required for each subcarrier. Hence, the Control Unit must send 2-bit word to appropriate I and Q Mapper. The system is thus capable of performing a different modulation technique for each subcarrier. The architecture of the implemented NCO shows the simplicity and flexibility of the subsystems. The main functional unit of this subsystem is the Phase Accumulator. This stage receives the clock and the TWN -Tuning Word assigned to the N sub-channel signals and goes through the entire count.

The major drawback of the architecture described in [5] is the use of NCO rather than the use of DUC, which increases the system latency and leads to the need of synchronization hardware.

## 4. DESIGN AND IMPLEMENTATION

### 4.1 Design Specification

It is necessary to clarify that the system being designed in this paper works inside a frequency limitation established by the FPGA. This means it will never be able to directly modify the value of the RF carrier frequency. However, if we add a typical RF frontend-with only one up-converter, it will be able to modify the RF carrier frequency to fit the transmission system requirements.

The table 1 details the design specifications. The maximum RF that can be fed to the SPARTAN 3 FPGA board is 500 MHz. The number of subcarriers chosen was 64, with the bandwidth of each subcarrier as 7.8 MHz. Cyclic prefix chosen is 25% of the number of subcarriers used. Modulation schemes used are QPSK and 16-QAM. The data rate achieved is 100 Mbps.

### 4.2 Design of Numerically Controlled Oscillator

The design consists of an oscillator based on direct digital synthesis (DDS) techniques. DDS techniques are defined as a digital control method of generating multiple frequencies from a reference clock signal. This provides a system with great accuracy in terms of signal integrity. The core of the DDS scheme, depicted in Figure 2, is the phase accumulator, which is basically a counter that increments its count value with every rising edge of the clock and represents the periodical characteristic of a sine wave. However, it is necessary to clarify that the increment is set by the Tuning Word signal, which has a word length of M bits. Thus, it is possible to vary the frequency by changing the Tuning Word value. The signal obtained from this stage becomes the memory address (M-bit word) of the lookup table.

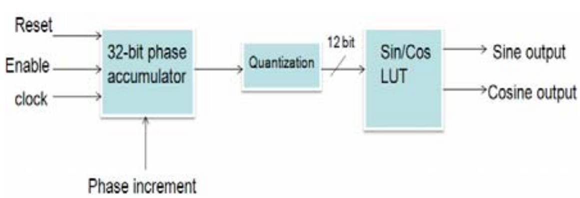


**Fig. 2 NCO architecture**

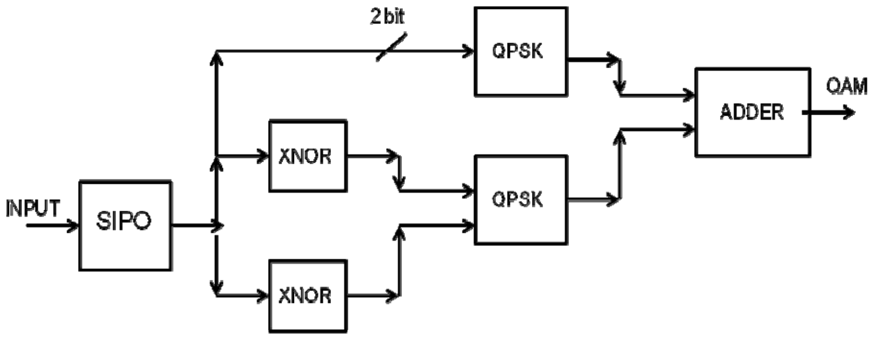


**Fig. 3 Block diagram of 16-QAM**

### 4.3Design of 16-QAM

The input to the QAM, shown in Figure 3, is fed through the Serial-in Parallel-out (SIPO) block. The 4-bit parallel data is then passed onto the two Quad Phase shift keying (QPSK) blocks. The first QPSK block is fed with the two MSB bits of the SIPO block, whereas the second QPSK is fed with the outputs of two XNOR gates. The outputs of the QPSK blocks are then fed to the adder where both of them are added to produce a 10- bit QAM output.

### 4.4 Design of re-configurable MIMO-OFDM module

The Figures 4 and 5 represent the simplified DFe MIMO-OFDM transmitter and receiver sections. The design depicted in this section was carried out utilizing the NCO to generate and map the modulated data onto subcarriers, unlike the conventional IFFT/FFT module based systems. The use of NCO not only ensures higher operating frequency, but also lowers resource utilization on an FPGA. In figure 4, the data arriving out of de-serializer is multiplied with the subcarriers generated from the NCO. These signals are then summed up. Next, the 16- point cyclic prefix is inserted before serializing the data to be transmitted. In figure 5, the transmitted OFDM signal is de-serialized before the cyclic prefix is removed. This data is then multiplied with the subcarrier frequencies generated by NCO to recover the modulated data. The modulated data is then fed to QPSK or 16- QAM demodulator to recover the input data.

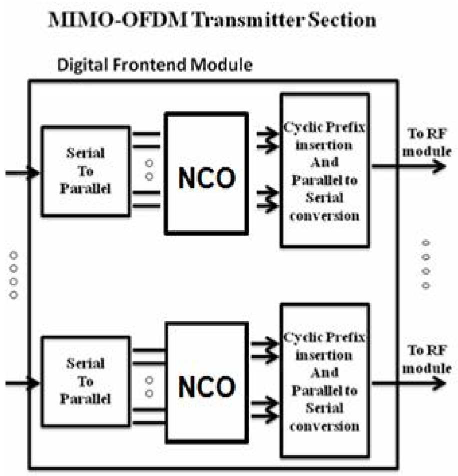


**Fig. 4 Simplified DFe MIMO-OFDM transmitter section**

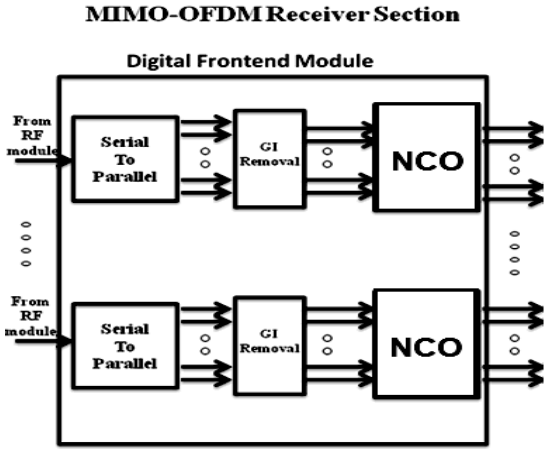


**Fig. 5 Simplified DFe MIMO-OFDM receiver section**

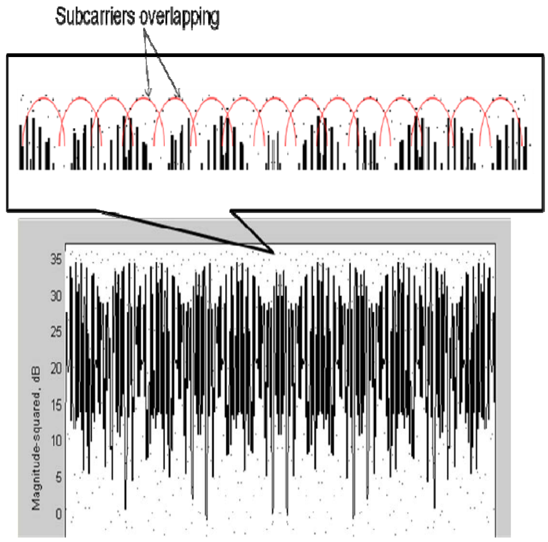


**Fig. 6 OFDM signal generated by the reference model**

The Figure 6 is the OFDM signal generated by the MIMO-OFDM reference module in MATLAB. The orthogonal overlapping of the subcarriers is illustrated in figure 6.

The figure 7 depicts the OFDM signal generated by the transmitter section, which indicates the orthogonal overlapping of the subcarriers. It also depicts the recovered input for varying input vectors.

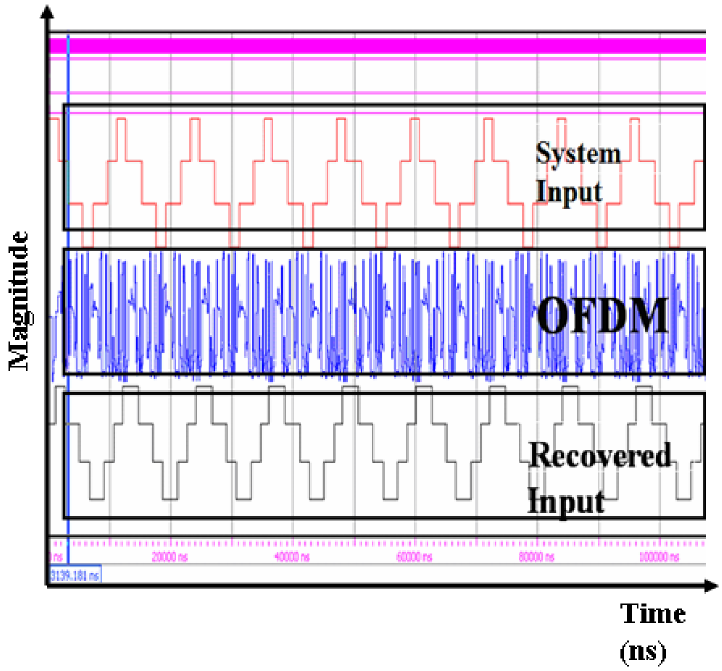


**Fig. 7 Simulation results of re-configurable MIMO-OFDM system**

## 5. VALIDATIONS AND DISCUSSION OF RESULTS

The Table 2 displays the resource utilization summary of the IFFT block versus the NCO after the synthesis process targeted for Virtex II board. The Virtex II board was targeted due to the fact IFFT occupied 143% of the LUT-FF pairs on SPARTAN 3 FPGA board. The results tabulated in table 2 clearly indicate that the use of NCO results in lesser resource utilization and also higher frequency of operation. The result also indicates that the NCO works 25% faster than the IFFT module.

**Table 2. IFFT vs. NCO resource utilization on Virtex II FPGA board**

| FPGA resources | Available resources | IFFT/ FFT | Utiliz-ation | NCO | Utiliz-ation |
|---|---|---|---|---|---|
| Slice Registers | 19200 | 1231 | 6% | 44 | 0.23% |
| Slice LUTs | 19200 | 971 | 5% | 34 | 0.17% |
| LUT-FF pairs | 1289 | 913 | 70% | 33 | 2.5% |
| Bonded IOBs | 220 | 4 | 1% | 83 | 37.7% |
| Block RAM | 32 | 0 | 0% | 3 | 9.3% |
| Max. frequency | | 372.75 MHz | | 469.39 MHz | |

Implementation of the re-configurable DFe MIMO-OFDM module had encountered a few challenges in the initial stages. They were overcome with the method listed in the following section.

The challenge that was encountered during this design was related to the frequency output that was generated out of the NCO. The designed NCO, initially, had a $2^{10}$ LUT entries. The output sine wave was then multiplied with either the QPSK or the QAM outputs.

At the receiver section of the DFe MIMO-OFDM module the recovered modulated signal was encountering data loss due to spectrally inferior subcarriers. This prompted the NCO to be redesigned with a $2^{12}$ entry LUT. The redesigned LUT had 12-bit sine wave generated out of it, leading to a spectrally improved wave being generated.

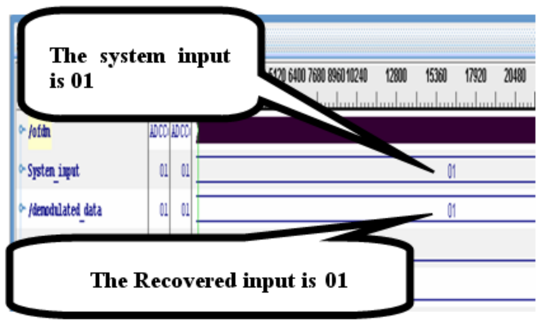


**Fig. 8 Behavior of the re-configurable DFe MIMO-OFDM module on Chipscope Pro**

- The Figure 8 illustrates the behavior of the re-configurable DFe MIMO-OFDM module hardware on the FPGA board using Chipscope Pro tool. Figure 8 depicts that the input fed to the system was '01'. It also depicts that the input fed to the system was successfully recovered at the receiver section.

## 6. CONCLUSION

- The switching between the two modulation schemes, QPSK and 16-QAM, aids in re-configurability of the system, based on the channel characteristics ensuring least possible transmission errors
- The benefits of the use of NCO are evident from the fact that the design was targeted and synthesized for a low end FPGA board with lower

resources, which would not be possible otherwise. The NCO based design utilized just 30% of the available slice on SPARTAN 3 FPGA board, whereas the IFFT based design requires 103% of it. This is a 70% reduction in resource utilization

- The maximum frequency achieved with NCO based design was 181MHz, whereas the IFFT based design operated at a maximum of 144MHz. The achieved frequency of operation was 25% higher than IFFT based design

The dynamic power of the NCO based architecture is 258.48 µW and leakage power at 20 µW, which is 10% lower than the IFFT based design.

## 7. REFERENCES

[1] Matthew Welborn, (2005) UWB System Design: Scaling Wireless Technology Across Data Rate Applications and Ranges, Texas Wireless Symposium.

[2] S.S.Riaz Ahamed, (2008) Performance analysis of OFDM, Journal of Theoretical and Applied Information Technology, 4, pp. 1- 6.

[3] Batra, A. Balakrishnan, J. Aiello, G.R. Foerster and J. R. Dabak, A, (2004) Design of a multiband OFDM system for realistic UWB channel environments, IEEE transactions on Communications, 52, pp. 2123 - 2138.

[4] W. Pam Siriwongpairat and K. J. Ray Liu, (2007) Ultra-Wideband Communications Systems: Multiband OFDM Approach, Wiley-IEEE Press, pp. 5 - 7.

[5] Oscar Robles Palacios and Carlos Silva Cardenas, (2008) Design and implementation of a reconfigurable OFDM modulator for software-defined radios, Proceedings of the IEEE International Conference of 4th Southern Programmable Logic, pp. 241 – 244.

[6] Walt Kester, and A. Abidi, (2005) Data Conversion Handbook, Newes publications, pp. 67.